Claim Amendments:

Claims 1-11 (canceled)

12. (currently amended) A vertical DRAM capacitor prepared by the process ~~of claim 1, and~~ of:

forming a deep trench (DT) etch in a substrate, depositing a first nitride layer on walls of the deep trench (DT), filling the trench with a sacrificial poly silicon, planarizing and poly recessing to obtain a depth above a later formed STI isolation;

depositing a dielectric layer different from said first nitride layer in the trench and depositing a second nitride thereon, thus forming a first nitride/dielectric layer/second nitride stack;

opening the dielectric layer and the second nitride in said trench by a RIE, and recessing the sacrificial trench poly to a depth that corresponds to a desired lower end of the collar and that defines the depth at which the bottle and buried plate are formed in a later processing step;

etching to remove the first nitride layer that was exposed during said recessing silicon sidewalls and to remove the second nitride layer from the stack and etching the silicon to:

create a recess large enough to place the collar oxide outside the trench; and

create a trench shape that allows uniform LOCOS oxidation;

affecting LOCOS oxidation that has an upper and lower limit due to said first and second nitride layers, and forms bird's beaks between the dielectric layer different from said nitride layer and said second nitride layer, said LOCOS oxide thickness being chosen to suppress vertical transistor action;

depositing a second mask layer system of nitride/ second dielectric layer to provide a layer on top of the LOCOS oxide for gas phase doping and to protect said second mask layer system during sacrificial poly strip;

affecting RIE to open the nitride/ second dielectric stack and the LOCOS oxide at the trench poly and stripping the sacrificial poly while protecting trench sidewalls by the nitride layer;

stripping nitride from the trench sidewall and from the mask, affecting on oxide etch, and preparing a bottle formation and gasphase doping such that said bottle formation and gasphase doping are self aligned;

depositing a node dielectric layer;

affecting a trench poly fill and poly recessing to create a position of a LOCOS oxide; and

etching the node dielectric, affecting a nitride etch to expose the trench sidewalls, affecting a buried strap nitridation of the silicon walls, affecting a buried strap poly deposition; planarizing and recessing to an upper position of the buried strap, and forming a trench top oxide (TTO); said vertical DRAM capacitor being characterized by: a buried collar fabricated after DT etch and before trench processing; self aligned bottle and gas phase doping; no consumption of silicon at the depth of the buried strap; and no reduction of trench diameter.

13. (currently amended) A vertical DRAM capacitor formed [[by]] according to the process of claim [[2.]] 12 wherein said dielectric layer different from said nitride layers is an oxide layer that serves as a mask for later processing.

14. (currently amended) A vertical DRAM capacitor formed [[by]] according to the process of claim [[3.]] 12 wherein said dielectric layer different from said first nitride layer is created by radical assisted oxidation.

15. (currently amended) A vertical DRAM capacitor formed [[by]] according to the process of claim [[4.]] 12 wherein said first and second nitride layers are deposited by LPCVD.

16. (currently amended) A vertical DRAM capacitor formed [[by]] according to the process of claim [[5.]] 13 wherein a second nitride layer is deposited on said dielectric layer, said second nitride layer serving to protect the oxide mask during sacrificial poly strip.

17. (currently amended) A vertical DRAM capacitor formed [[by]] according to the process of claim [[6.]] 12 wherein after the nitride etch the oxide mask is stripped.

18. (currently amended) A vertical DRAM capacitor formed [[by]] according to the process of claim [[7.]] 16 wherein said LOCOS oxide thickness that suppresses vertical parasitic transistor action is about 300A.

19. (currently amended) A vertical DRAM capacitor formed [[by]] according to the process of claim [[8.]] 18 wherein said LOCOS oxidation is thermal oxidation at temperatures between 1,000°C to about 1,200°C to assure uniform oxide thickness.

20. (currently amended) A vertical DRAM capacitor formed [[by]] according to the process of claim [[9.]] 12 wherein said second dielectric layer is an oxide.

21. (currently amended) A vertical DRAM capacitor formed [[by]] according to the process of claim [[10.]] 20 wherein a RIE is used to open the second mask layer system.

22. (currently amended) A vertical DRAM capacitor formed [[by]] according to the process of claim [[11.]] 21 wherein said node dielectric is a node nitride.